## MB39C007

## PIN ASSIGNMENT



■ PIN DESCRIPTIONS

| Pin No. | Pin Name | I/O | Description |
| :---: | :---: | :---: | :--- |
| 1 | CTLP | I | Voltage detection circuit block control input pin. <br> (L: Voltage detection function stop / H : Normal operation) |
| 2,3 | CTL2, CTL1 | I | DC/DC converter block control input pins. <br> (L: Shut down / H : Normal operation) |
| 4 | AGND |  | Control block ground pin. |
| 5 | AVDD |  | Control block power supply pin. |
| 6 | VREF | O | Reference voltage output pin. |
| 7 | VDET | I | Voltage detection input pin. |
| 8,23 | VREFIN1, VREFIN2 | I | Error amplifier (Error Amp) non-inverted input pins. |
| 9,22 | MODE1, MODE2 | I | Operation mode switch pins. <br> (L : PFM/PWM mode / OPEN : PWM mode) |
| 10,21 | OUT1, OUT2 | I | Output voltage feedback pins. |
| 11,12 | DVDD1 |  | Drive block power supply pins. |
| 19,20 | DVDD2 |  | Inductor connection output pins. <br> High impedance during shut down. |
| 13,18 | LX1, LX2 |  | Drive block ground pins. |
| 14,15 | DGND1 | O | VDET circuit output pin. <br> Connected to an N-ch MOS open drain circuit. |
| 16,17 | DGND2 | XPOR |  |

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## I/O PIN EQUIVALENT CIRCUIT DIAGRAM



## BLOCK DIAGRAM



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## Current mode

- Original voltage mode type :

Stabilize the output voltage by comparing two items below and on-duty control.

- Voltage (Vc) obtained through negative feedback of the output voltage by Error Amp
- Reference triangular wave ( $\mathrm{V}_{\text {TRI }}$ )
- Current mode type :

Instead of the triangular wave ( $\mathrm{V}_{\text {TRII }}$ ), the voltage ( $\mathrm{V}_{\text {IIETT }}$ ) obtained through I-V conversion of the sum of currents that flow in the oscillator (rectangular wave generation circuit) and SW FET is used.
Stabilize the output voltage by comparing two items below and on-duty control.

- Voltage (Vc) obtained through negative feedback of the output voltage by Error Amp
- Voltage (VIDET) obtained through I-V conversion of the sum of current that flow in the oscillator (rectangular wave generation circuit) and SW FET



## FUNCTION OF EACH BLOCK

- PFM/PWM Logic control circuit

In normal operation, frequency ( 2.0 MHz ) which is set by the built-in oscillator (square wave oscillation circuit) controls the built-in P-ch MOS FET and N-ch MOS FET for the synchronous rectification operation. In the light load mode, the intermittent (PFM) operation is executed.
This circuit protects against pass-through current caused by synchronous rectification and against reverse current caused in a non-successive operation mode.

- lout Comparator circuit

This circuit detects the current (lLx) which flows to the external inductor from the built-in P-ch MOS FET.
By comparing VIDET obtained through I-V conversion of peak current Ipk of ILx with the Error Amp output, the builtin P-ch MOS FET is turned off via the PFM/PWM Logic Control circuit.

- Error Amp phase compensation circuit

This circuit compares the output voltage to reference voltages such as VREF. This IC has a built-in phase compensation circuit that is designed to optimize the operation of this IC.
This needs neither to be considered nor addition of a phase compensation circuit and an external phase compensation device.

- VREF circuit

A high accuracy reference voltage is generated with BGR (bandgap reference) circuit. The output voltage is 1.30 V (Typ).

- Voltage Detection (VDET) circuit

The voltage detection circuit monitors the VDET pin voltage. Normally, use the XPOR pin through pull-up with an external resistor. When the VDET pin voltage reaches 0.6 V , it reaches the H level.

Timing chart example : (XPOR pin pulled up to Viv)


## - Protection circuit

This IC has a built-in over-temperature protection circuit.
The over-temperature protection circuit turns off both N -ch and P -ch switching FETs when the junction temperature reaches $135 \quad \mathrm{C}$. When the junction temperature comes down to $110 \quad \mathrm{C}$, the switching FET is returned to the normal operation. Since the PFM/PWM control circuit of this IC is in the control method in current mode, the current peak value is also monitored and controlled as required.

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- Function table

| Input |  |  |  | Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CTL1 | CTL2 | CTLP | MODE | CH1 function | CH2 function | VDET function | VREF function | Switching operation |
| L |  |  | * | Stopped |  |  |  |  |
| H | L | L | L | Operation | Stopped | Stopped | 1.3 V output | PFM/PWM mode |
| L | H |  |  | Stopped | Operation |  |  |  |
| H |  |  |  | Operation |  |  |  |  |
| L |  | H |  | Stopped |  | Operation |  |  |
| H | L |  |  | Operation | Stopped |  |  |  |
| L | H |  |  | Stopped | Operation |  |  |  |
| H |  |  |  | Operation |  |  |  |  |
| H | L | L | Open | Operation | Stopped | Stopped |  | PWM fixed mode |
| L | H |  |  | Stopped | Operation |  |  |  |
| H |  |  |  | Operation |  |  |  |  |
| L |  | H |  | Stopped |  | Operation |  |  |
| H | L |  |  | Operation | Stopped |  |  |  |
| L | H |  |  | Stopped | Operation |  |  |  |
| H |  |  |  | Operation |  |  |  |  |

[^0]RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Power supply voltage | Vdo | AVDD DVDD1 DVDD2 | 2.5 | 3.7 | 5.5 | V |
| VREFIN voltage | Vrefin |  | 0.15 |  | 1.30 | V |
| CTL voltage | Vctı | CTLP, CTL1, CTL2 pins | 0 |  | 5.0 | V |
| LX current | ILx | ILx1, ILx2 |  |  | 800 | mA |
| VREF output current | Irout | $\begin{aligned} & \text { 2.5 V AVDD DVDD1 } \\ & \text { DVDD2 } 3.0 \mathrm{~V} \end{aligned}$ |  |  | 0.5 | mA |
|  |  | $\begin{array}{\|l\|l\|} \hline \text { 3.0 V AVDD } & \text { DVDD1 } \\ \text { DVDD2 } 5.5 \mathrm{~V} & \\ \hline \end{array}$ |  |  | 1 |  |
| XPOR current | Ipor |  |  |  | 1 | mA |
| Inductor value | L |  |  | 2.2 |  | H |

Note : The output current from this device has a situation to decrease if the power supply voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) and the $\mathrm{DC} / \mathrm{DC}$ converter output voltage (VOut) differ only by a small amount. This is a result of slope compensation and will not damage this device.
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(Ta 25 C , AVDD DVDD1 DVDD2 3.7 V , VOUT1/VOUT2 setting value 2.5 V , MODE1/MODE2 0 V )

| Parameter |  | Symbol | Pin No. | Condition | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| DC/DC converter block | Input current |  | IREFIN | 8,23 | VREFIN 0.15 V to 1.3 V | 100 | 0 | 100 | nA |
|  | Output voltage | Vout | 10, 21 | VREFIN 0.833 V , OUT 100 mA | 2.45 | 2.50 | 2.55 | V |
|  | Input stability | LINE |  | $\begin{aligned} & \text { 2.5 V AVDD } \quad \text { DVDD1 } \\ & \text { DVDD2 } 5.5 \mathrm{~V}^{*}{ }_{1} \end{aligned}$ |  |  | 10 | mV |
|  | Load stability | LOAD |  | 100 mA OUT 800 mA |  |  | 10 | mV |
|  | OUT pin input impedance | Rout |  | OUT 2.0 V | 0.6 | 1.0 | 1.5 | M |
|  | LX Peak current | IPk | 13, 18 | Output shorted to GND | 0.9 | 1.2 | 1.7 | A |
|  | PFM/PWM switch current | Imsw |  |  |  | 30 |  | mA |
|  | Oscillation frequency | fosc |  |  | 1.6 | 2.0 | 2.4 | MHz |
|  | Rise delay time | tpg | $\begin{gathered} 2,3, \\ 10,21 \end{gathered}$ | C1/C2 4.7 F, OUT 0 A, <br> OUT1/OUT2 : 0 90 <br> Vout  |  | 45 | 80 | s |
|  | SW NMOS-FET OFF voltage | V NoFF | 13, 18 |  |  | 10* |  | mV |
|  | SW PMOS-FET <br> ON resistance | Ronp |  | LX1/LX2 100 mA |  | 0.30 | 0.48 |  |
|  | SW NMOS-FET ON resistance | Ronn |  | LX1/LX2 100 mA |  | 0.20 | 0.42 |  |
|  | LX leak current | ILEakm |  | 0 LX $\mathrm{V}^{\text {DD }}$ 2 | 1.0 |  | 8.0 | A |
|  |  | ILEAKH |  | VDD 5.5 V, 0 LX V $\mathrm{Do}^{* 2}$ | 2.0 |  | 16.0 | A |
| Protection circuit block | Overheating protection (Junction Temp.) | TOTPH |  |  | 120* | 135* | 160* | C |
|  |  | TотPL |  |  | 95* | 110* | 125* | C |
|  | UVLO threshold | $\mathrm{V}_{\text {тнниv }}$ | $\begin{gathered} 5,11, \\ 12,19, \\ 20 \end{gathered}$ |  | 2.17 | 2.30 | 2.43 | V |
|  | voltage | $\mathrm{V}_{\text {thluv }}$ |  |  | 2.03 | 2.15 | 2.27 | V |
|  | UVLO hysteresis width | Vhrsuv |  |  | 0.08 | 0.15 | 0.25 | V |
| Voltage detection circuit block | XPOR threshold | $\mathrm{V}_{\text {TH }} \mathrm{V}_{\text {IfR }}$ | 7 |  | 575 | 600 | 625 | mV |
|  | voltage | $\mathrm{V}_{\text {THLPR }}$ |  |  | 558 | 583 | 608 | mV |
|  | XPOR hysteresis width | VhYSPR |  |  |  | 17 |  | mV |
|  | XPOR output voltage | VoL | 24 | XPOR 25 A |  |  | 0.1 | V |
|  | XPOR output current | Іон |  | XPOR 5.5 V |  |  | 1.0 | A |

* : This value is not be specified. This should be used as a reference to support designing the circuits.
(Continued)


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(Continued)
(Ta 25 C, AVDD DVDD1 DVDD2 3.7 V , VOUT1/VOUT2 setting value 2.5 V , MODE1/MODE2 0 V )

| Parameter |  | Symbol | Pin No. | Condition | Value |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  |  | Typ | Max |  |
| Control block | CTL threshold voltage |  | V тнНст | 1, 2, 3 |  | 0.55 | 0.95 | 1.45 | V |
|  |  | $\mathrm{V}_{\text {thlct }}$ |  |  | 0.40 | 0.80 | 1.30 | V |
|  | CTL pin input current | lictl | $\begin{aligned} & \hline 0 \mathrm{~V} \text { CTLP/CTL1/CTL2 } \\ & 3.7 \mathrm{~V} \end{aligned}$ |  |  |  | 1.0 | A |
| Reference voltage block | VREF voltage | V ReF | 6 | VREF 0 A | 1.274 | 1.300 | 1.326 | V |
|  | VREF Load stability | Loadref |  | VREF 1.0 mA |  |  | 20 | mV |
| General | Shut down power supply current | Ivod1 | $\begin{gathered} 5,11, \\ 12,19, \\ 20 \end{gathered}$ | CTLP/CTL1/CTL2 0 V , State of all circuits OFF*3 |  |  | 1.0 | A |
|  |  | Ivdoth |  | CTLP/CTL1/CTL2 0 V , <br> Vod 5.5 V , <br> State of all circuits OFF*3 |  |  | 1.0 | A |
|  | Power supply current at DC/DC operation 1 (PFM mode) | Ivod21 |  | 1. CTLP $0 \mathrm{~V}, \mathrm{CTL} 13.7 \mathrm{~V}$, CTL2 0 V <br> 2. CTLP $0 \mathrm{~V}, \mathrm{CTL} 10 \mathrm{~V}$, CTL2 3.7 V, OUT 0 A |  | 30 | 48 | A |
|  |  | Ivdo22 |  | $\begin{aligned} & \text { CTLP 0 V, CTL1/CTL2 } \\ & 3.7 \mathrm{~V}, \text { OUT } 0 \mathrm{~A} \\ & \hline \end{aligned}$ |  | 50 | 80 | A |
|  | Power supply current at DC/DC operation 2 (PWM mode) | Ivod31 |  | 1. CTLP 0V, CTL1 3.7 V , CTL2 0 V, MODE1/ MODE2 OPEN <br> 2. CTLP $0 \mathrm{~V}, \mathrm{CTL} 10 \mathrm{~V}$, CTL2 3.7 V , MODE1/ MODE2 OPEN, OUT OA |  | 3.5 | 10.0 | mA |
|  |  | IvdD32 |  | ```CTLP 0 V, CTL1/CTL2 3.7 V, MODE1/MODE2 OPEN, OUT O A``` |  | 7.0 | 20.0 | mA |
|  | Power supply current (voltage detection mode) | Ivod5 |  | $\begin{aligned} & \text { CTLP } 3.7 \mathrm{~V}, \\ & \text { CTL1/CTL2 } 0 \mathrm{~V} \end{aligned}$ |  | 15 | 24 | A |
|  | Power-on invalid current | Ivod |  | 1. CTL1 3.7 V, CTL2 0 V <br> 2. CTL1 $0 \mathrm{~V}, \mathrm{CTL} 23.7 \mathrm{~V}$, VOUT1/VOUT2 90 , OUT $0 A^{*} 4$ |  | 1000 | 2000 | A |

*1 : The minimum value of AVDD DVDD1 DVDD2 is the 2.5 V or V out setting value +0.6 V , whichever is higher.
*2 : The leak at the LX pin includes the current of the internal circuit.
*3 : Sum of the current flowing into the AVDD, the DVDD1, and the DVDD2 pins.
*4 : Current consumption based on $100 \%$ ON-duty (High side FET in full ON state). The SW FET gate drive current is not included because the device is in full ON state (no switching operation). Also the load current is not included.

## TEST CIRCUIT FOR MEASURING TYPICAL OPERATING CHARACTERISTICS



| Component | Specification | Vendor | Part Number | Remarks |
| :---: | :---: | :---: | :---: | :--- |
| R1 | 1 M | KOA | RK73G1JTTD D 1 M |  |
| R3-1 | 20 k | SSM | RR0816-203-D | VOUT1/VOUT2 2.5 V |
| R3-2 | 150 k | SSM | RR0816-154-D |  |
| R4 | 300 k | SSM | RR0816-304-D |  |
| R5 | 510 k | KOA | RK73G1JTTD D510 k |  |
| R6 | 100 k | SSM | RR0816-104-D |  |
| C1 | 4.7 F | TDK | C2012JB1A475K |  |
| C2 | 4.7 F | TDK | C2012JB1A475K |  |
| C3 | 0.1 F | TDK | C1608JB1E104K |  |
| C6 | 0.1 F | TDK | C1608JB1H104K | For adjusting slow start time |
| L1 | 2.2 H | TDK | VLF4012AT-2R2M |  |

Note : These components are recommended based on the operating tests authorized.
TDK : TDK Corporation
SSM : SUSUMU Co., Ltd
KOA : KOA Corporation

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## [2] Output voltage setting

The output voltage Vout (Vout1 or Voutr) of this IC is defined by the voltage input to VREFIN (VREFIN1 or VREFIN2). Supply the voltage for inputting to VREFIN from an external power supply, or set the VREF output by dividing it with resistors.
The output voltage when the VREFIN voltage is set by dividing the VREF voltage with resistors is obtained by the following formula.

Vout $2.97 V_{\text {refin, }} \quad V_{\text {refin }} \frac{R 2}{R 1 \quad R 2} \quad V_{\text {ref }}$
(VReF 1.30 V )


Note : Refer to "■ APPLICATION CIRCUIT EXAMPLES" for the an example of this circuit.
Although the output voltage is defined according to the dividing ratio of resistance, select the resistance value so that the current flowing through the resistance does not exceed the VREF current rating ( 1 mA ).

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## [3] About conversion efficiency

The conversion efficiency can be improved by reducing the loss of the DC/DC converter circuit. The total loss (PLoss) of the DC/DC converter is roughly divided as follows :

Ploss P cont P sw P c

Pcont : Control system circuit loss (The power used for this IC to operate, including the gate driving power for internal SW FETs)
Psw : Switching loss (The loss caused during switching of the IC's internal SW FETs)
Pc : Continuity loss (The loss caused when currents flow through the IC's internal SW FETs and external circuits )
The IC's control circuit loss (Pcont) is extremely small, less than $100 \mathrm{~mW}^{*}$ (with no load).
As the IC contains FETs which can switch faster with less power, the continuity loss ( Pc ) is more predominant as the loss during heavy-load operation than the control circuit loss (Pcont) and switching loss (Psw).
Furthermore, the continuity loss $\left(\mathrm{P}_{\mathrm{c}}\right)$ is divided roughly into the loss by internal SW FET ON-resistance and by external inductor series resistance.
Pc I out ${ }^{2}$ (RDC
D Ronp (1
D) Ronn)
D : Switching ON-duty cycle ( V out / Vin)
Ronp : Internal P-ch SW FET ON resistance
Ronn : Internal N-ch SW FET ON resistance
RDC : External inductor series resistance
lout : Load current

The above formula indicates that it is important to reduce RDC as much as possible to improve efficiency by selecting components.
*: The loss in the successive operation mode. This IC suppresses the loss in order to execute the PFM operation in the low load mode (less than 100 A in no load mode). Mode is changed by the current peak value lpk which flows into switching FET. The threshold value is about 30 mA .

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## [4] Power dissipation and heat considerations

The IC is so efficient that no consideration is required in most cases. However, if the IC is used at a low power supply voltage, heavy load, high output voltage, or high temperature, it requires further consideration for higher efficiency.
The internal loss $(\mathrm{P})$ is roughly obtained from the following formula :

P lout $^{2}$ (D Ronp (1 D) R onn)

D : Switching ON-duty cycle ( V out / Vin)
Ronp : Internal P-ch SW FET ON resistance
Ronn : Internal N-ch SW FET ON resistance
lout : Output current

The loss expressed by the above formula is mainly continuity loss. The internal loss includes the switching loss and the control circuit loss as well but they are so small compared to the continuity loss they can be ignored.

In this IC with Ronp greater than Rons, the larger the on-duty cycle, the greater the loss.

When assuming $\mathrm{V}_{\mathrm{IN}} 3.7 \mathrm{~V}$, Ta 70 C , for example, Ronp 0.36 and Ronn 0.30 according to the graph "MOS FET ON resistance vs. Operating ambient temperature". The IC's internal loss P is 123 mW at Vout 2.5 V and lout 0.6 A . According to the graph "Power diss ipation vs. Operating ambient temperature", the power dissipation at an operating ambient temperature Ta of $70 \quad \mathrm{C}$ is 300 mW and the internal loss is smaller than the power dissipation.

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## [5] XPOR threshold voltage setting [VPORH, $\mathrm{V}_{\text {PORL }}$ ]

Set the detection voltage by applying voltage to the VDET pin via an external resistor calculated according to this formula.
$V_{\text {PORH }} \frac{R 3 R 4}{R 4} \quad V_{\text {thHPR }}$

$V_{\text {therp }} 0.600 \mathrm{~V}$
$V_{\text {thlpr }} 0.583 \mathrm{~V}$
Example for setting detection voltage to 3.7 V
R3 510 k
R4 100 k


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## [6] Transient response

Normally, lout is suddenly changed while $\mathrm{V}_{\mathrm{In}}$ and Vout are maintained constant, responsiveness including the response time and overshoot/undershoot voltage is checked. As this IC has built-in Error Amp with an optimized design, it shows good transient response characteristics. However, if ringing upon sudden change of the load is high due to the operating conditions, add capacitor C6 (e.g. $0.1 \quad$ F). (Since this capacitor C 6 changes the start time, check the start waveform as well.) This action is not required for DAC input.


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## [7] Board layout, design example

The board layout needs to be designed to ensure the stable operation of this IC.
Follow the procedure below for designing the layout.

- Arrange the input capacitor (Cin) as close as possible to both the VDD and GND pins. Make a through-hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- Large AC currents flow between this IC and the input capacitor (Cin), output capacitor (Co), and external inductor (L). Group these components as close as possible to this IC to reduce the overall loop area occupied by this group. Also try to mount these components on the same surface and arrange wiring without throughhole wiring. Use thick, short, and straight routes to wire the net (The layout by planes is recommended.).
- Arrange a bypass capacitor for AVDD as close as possible to both the ADVV and AGND pins. Make a through-hole (TH) near the pins of this capacitor if the board has planes for power and GND.
- The feedback wiring to the OUT should be wired from the voltage output pin closest to the output capacitor (Co). The OUT pin is extremely sensitive and should thus be kept wired away from the LX pin of this IC as far as possible.
- If applying voltage to the VREFIN1/VREFIN2 pins through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange them so that the GND pin of VREFIN1/VREFIN2 resistor is close to the IC's AGND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current. If installing a bypass capacitor for the VREFIN, put it close to the VREFIN pin.
- If applying voltage to the VDET pin through dividing resistors, arrange the resistors so that the wiring can be kept as short as possible. Also arrange so that the GND pin of the VDET resistor is close to the IC's AGND pin. Further, provide a GND exclusively for the control line so that the resistor can be connected via a path that does not carry current.
- Try to make a GND plane on the surface to which this IC will be mounted. For efficient heat dissipation when using the QFN- 24 package, FUJITSU MICROELECTRONICS recommends providing a thermal via in the footprint of the thermal pad.
Example of arranging IC SW system parts



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## EXAMPLE OF STANDARD OPERATION CHARACTERISTICS

(Shown below is an example of characteristics for connection according to "四TEST CIRCUIT FOR MEASURING TYPICAL OPERATING CHARACTERISTICS".)

- Characteristics CH1

(Continued)

(Continued)


## MB39C007


(Continued)

(Continued)

## MB39C007


(Continued)


## MB39C007


(Continued)
(Continued)


- Switching waveform

PFM/PWM operation

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{IO} 1=5 \mathrm{~mA}, \mathrm{~V} 01=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

PWM operation

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO} 1=2.5 \mathrm{~V}, \mathrm{IO} 1=800 \mathrm{~mA}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{IO}=5 \mathrm{~mA}, \mathrm{~V}$ O2 $=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{Vo2}=1.8 \mathrm{~V}, \mathrm{IO} 2=800 \mathrm{~mA}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

- Output waveforms at sudden load changes

$$
0 \mathrm{~A} \quad 800 \mathrm{~mA}
$$


$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO}=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

## $20 \mathrm{~mA} \quad 800 \mathrm{~mA}$


$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO1}=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$
$100 \mathrm{~mA} \quad 800 \mathrm{~mA}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO1}=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{Vo2}=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO2}=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO2}=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=25 \mathrm{C}$

- CTL start-up waveform

No load, No VREFIN capacitor

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO1}=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=+25 \mathrm{C}$


V IN $=3.7 \mathrm{~V}, \mathrm{VO}=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=+25 \mathrm{C}$

$\mathrm{V} I \mathrm{~N}=3.7 \mathrm{~V}, \mathrm{VO}=1.8 \mathrm{~V}, \mathrm{IO}=800 \mathrm{~mA}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=+25 \mathrm{C}$
(Continued)
(Continued)


## - CTL stop waveform

Maximum load, VREFIN capacitor 0.1 F

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO} 1=2.5 \mathrm{~V}, \mathrm{IO} 1=800 \mathrm{~mA}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=+25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO} 2=1.8 \mathrm{~V}, \mathrm{IO} 2=800 \mathrm{~mA}, \mathrm{MODE}=\mathrm{L}, \mathrm{Ta}=+25 \mathrm{C}$

- Current limitation waveform

$\mathrm{V} I \mathrm{~N}=3.7 \mathrm{~V}, \mathrm{VO1}=2.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{OPEN}, \mathrm{Ta}=25 \mathrm{C}$

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{VO} 2=1.8 \mathrm{~V}, \mathrm{MODE}=\mathrm{OPEN}, \mathrm{Ta}=25 \mathrm{C}$
- Voltage detection waveform

$\mathrm{VIN}=3.7 \mathrm{~V}, \mathrm{CTLP}=\mathrm{Vin}, \mathrm{Ta}=25 \mathrm{C}$
Pull-up XPOR to Vin at 1 k .


## - Waveform of dynamic output voltage transition (Vo1 $1.8 \mathrm{~V} \quad 2.5 \mathrm{~V}$ )



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## APPLICATION CIRCUIT EXAMPLES

## - APPLICATION CIRCUIT EXAMPLE 1

- An external voltage is input to the reference voltage external input (VREFIN1, VREFIN2), and the Vout voltage is set to 2.97 times the Vout setting gain.



## MB39C007

- APPLICATION CIRCUIT EXAMPLE 2
- The voltage of VREF pin is input to the reference voltage external input (VREFIN1, VREFIN2) by dividing resistors. The Vout1 voltage is set to 2.5 V and Vout2 voltage is set to 1.8 V .

- APPLICATION CIRCUIT EXAMPLE COMPONENTS LIST

| Component | Item | Part Number | Specification | Package | Vendor |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L1 | Inductor | VLF4012AT-2R2M | 2.2 H, RDC 76 m | SMD | TDK |
|  |  | MIPW3226D2R2M | 2.2 H, RDC 100 m | SMD | FDK |
| L2 | Inductor | VLF4012AT-2R2M | 2.2 H, RDC 76 m | SMD | TDK |
|  |  | MIPW3226D2R2M | 2.2 H, RDC 100 m | SMD | FDK |
| C1 | Ceramic capacitor | C2012JB1A475K | $4.7 \mathrm{~F}(10 \mathrm{~V})$ | 2012 | TDK |
| C2 | Ceramic capacitor | C2012JB1A475K | $4.7 \mathrm{~F}(10 \mathrm{~V})$ | 2012 | TDK |
| C3 | Ceramic capacitor | C2012JB1A475K | $4.7 \mathrm{~F}(10 \mathrm{~V})$ | 2012 | TDK |
| C4 | Ceramic capacitor | C2012JB1A475K | $4.7 \mathrm{~F}(10 \mathrm{~V})$ | 2012 | TDK |
| C5 | Ceramic capacitor | C1608JB1E104K | $0.1 \mathrm{~F}(50 \mathrm{~V})$ | 2012 | TDK |
| R1 | Resistor | RK73G1JTTD D 13 k RK73G1JTTD D 150 k | $\begin{aligned} & \hline 13 \mathrm{k} \\ & 150 \mathrm{k} \end{aligned}$ | $\begin{aligned} & 1608 \\ & 1608 \end{aligned}$ | $\begin{aligned} & \hline \text { KOA } \\ & \text { KOA } \end{aligned}$ |
| R2 | Resistor | RK73G1JTTD D 300 k | 300 k | 1608 | KOA |
| R5 | Resistor | RK73G1JTTD D 13 k RK73G1JTTD D 330 k | $\begin{aligned} & \hline 13 k \\ & 330 k \end{aligned}$ | $\begin{aligned} & 1608 \\ & 1608 \end{aligned}$ | $\begin{aligned} & \hline \text { KOA } \\ & \text { KOA } \end{aligned}$ |
| R6 | Resistor | RK73G1JTTD D 300 k | 300 k | 1608 | KOA |
| R7 | Resistor | RK73G1JTTD D 1 M | $1 \mathrm{M} \quad 0.5$ | 1608 | KOA |
| R8 | Resistor | RK73G1JTTD D 1 M | $1 \mathrm{M} \quad 0.5$ | 1608 | KOA |

TDK : TDK Corporation
FDK : FDK Corporation
KOA : KOA Corporation

## MB39C007

## USAGE PRECAUTIONS

## 1. Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions adversely affect the reliability of the LSI.
2. Use the devices within recommended operating conditions

The recommended operating conditions are the conditions under which the LSI is guaranteed to operate.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.
3. Printed circuit board ground lines should be set up with consideration for common impedance
4. Take appropriate static electricity measures

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 k to 1 M between body and ground.

5. Do not apply negative voltages

The use of negative voltages below 0.3 V may create parasitic transisto rs on LSI lines, which can cause abnormal operation.

## ORDERING INFORMATION

| Part number | Package | Remarks |
| :---: | :---: | :---: |
| MB39C007QN | 24-pin plastic QFN <br> (LCC-24P-M09) |  |

## ■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of FUJITSU MICROELECTRONICS with "E1" are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE).

A product whose part number has trailing characters "E1" is RoHS compliant.

## MB39C007

■ MARKING FORMAT (LEAD FREE VERSION)


## MB39C007

## LABELING SAMPLE (LEAD FREE VERSION)



## RECOMMENDED MOUNTING CONDITIONS OF MB39C007QN

[FUJITSU MICROELECTRONICS Recommended Mounting Conditions]

| Item | Condition |  |
| :---: | :---: | :---: |
| Mounting Method | IR (infrared reflow), warm air reflow |  |
| Mounting times | 2 times |  |
| Storage period | Before openingFromening to the 2nd <br> reflow | Please use it within two years after manufacture. |
| Storage conditions | 5 C to $30 \mathrm{C}, 70$ RH or less (the lowest possible humidity) |  |

## [Parameters for Each Mounting Method]

 IR (infrared reflow)260 C
C C

## EVALUATION BOARD SPECIFICATION

The MB39C007 Evaluation Board provides the proper for evaluating the efficiency and other characteristics of the MB39C007.

- Terminal information

| Symbol | Functions |
| :---: | :---: |
| VIN | Power supply terminal <br> In standard condition 3.1 V to $5.5 \mathrm{~V}^{*}$ <br> *: When the VIN/VOUT difference is to be held within 0.6 V or less, such as for devices with a standard output voltage (VOUT1 2.5 V ) when VIN < 3.1 V , FUJITSU MICROELECTRONICS recommends changing the output capacity (C1, C2) to 10 F . |
| VOUT1, VOUT2 | Output terminals <br> (VOUT1: CH1, VOUT2: CH2) |
| VCTL | Power supply terminal for setting the CTL1, CTL2 and CTLP terminals. Use by connecting with VIN (When SW is mounted). |
| CTL1, CTL2 | Direct supply terminal of CTL (CTL1 : for CH1, CTL2 : for CH2) CTL1, CTL2 0 V to 0.8 V (Typ.) : Shutdown CTL1, CTL2 0.95 V (Typ.) to $\mathrm{V} \operatorname{IN}(5 \mathrm{~V}$ Max) : Normal operation |
| MODE1, MODE2 | Direct supply terminal of MODE (CH1 : for MODE1, CH2 : for MODE2) MODE1, MODE2 0 V to 0.4 V (Max) PFM/PWM mode MODE1, MODE2 OPEN(Remove R1 and R4) : PWM mode |
| VREF | Reference voltage output terminal VREF 1.30 V (Typ.) |
| VREFIN1, VREFIN2 | External reference voltage input terminals <br> (VREFIN1 : for CH1, VREFIN2 : for CH2) <br> When an external reference voltage is supplied, connect it to the terminal for each channel. |
| VDET | Voltage input terminal for voltage detection |
| CTLP | Voltage detection circuit block control terminal CTLP L : Voltage detection circuit block stop CTLP H: Normal operation |
| XPOR | Voltage detection circuit output terminal The N-ch MOS open drain circuit is connected. |
| VXPOR | Pull-up voltage terminal for the XPOR terminal |
| PGND | Ground terminal Connect power supply GND to the PGND terminal next to the VIN terminal. Connect output (load) GND to the PGND terminal between the VOUT1 terminal and the VOUT2 terminal. |
| AGND | Ground terminal |

- Startup terminal information

| Terminal name | Condition | Functions |
| :---: | :--- | :--- |
| CTL1 | L : Open <br> H : Connect to VIN | ON/OFF switch for CH1 <br> L : Shutdown <br> H : Normal operation. |
| CTL2 | L : Open <br> H: Connect to VIN | ON/OFF switch for CH2 <br> L: Shutdown <br> H : Normal operation. |
| CTLP | L : Open <br> H : Connect to VIN | ON/OFF switch for the voltage detection block <br> L: Stops the voltage detection circuit <br> H: Normal operation. |

- Jumper information

| JP | Functions |
| :---: | :--- |
| JP1 | Short-circuited in the layout pattern of the board (normally used shorted). |
| JP2 | Short-circuited in the layout pattern of the board (normally used shorted). |
| JP3 | Not mounted |
| JP6 | Normally used shorted $\left(\begin{array}{ll}0 & ) \\ \hline\end{array}\right.$ |

## - Setup and checkup

(1) Setup

1. Connect the CTL1 terminal and the CTL2 terminal to the VIN terminal.
2. Put it into "L" state by connecting the CTLP terminal to the AGND pad.
3. Connect the power supply terminal to the VIN terminal, and the power supply GND terminal to the PGND terminal. Make sure PGND is connected to the PGND terminal next to the VIN terminal.
(Example of setting power-supply voltage : 3.7 V)
(2) Checkup

Supply power to VIN. The IC is operating normally if VOUT1 $=2.5 \mathrm{~V}$ (Typ) and VOUT2 $=1.8 \mathrm{~V}$ (Typ).

## MB39C007

- Component layout on the evaluation board (Top View)



## MB39C007

- Evaluation board layout (Top View)


Top Side (Layer1)


Inside VIN \& GND (Layer3)


Inside GND (Layer2)


Bottom Side (Layer4)

## PACKAGE DIMENSION

| 24-pin plastic QFN | Lead pitch | 0.50 mm |
| :--- | :--- | :--- |
|  | Sealing method | Plastic mold |
| (LCC-24P-M09) |  |  |

24-pin plastic QFN
(LCC-24P-M09)

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/

MEMO


[^0]:    * : Don't care

